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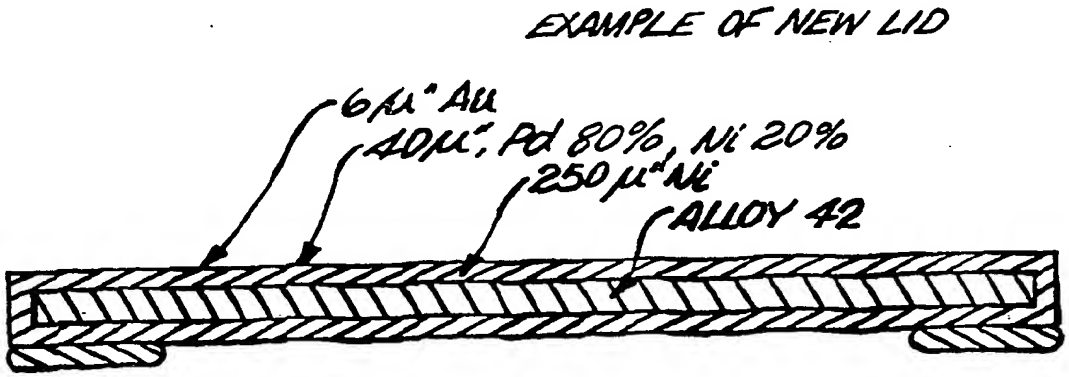

(57) Abstract

A solderable metallic cover for hermetically sealing a ceramic package that includes an iron or iron-alloy core and layers of nickel or nickel alloy on the core and palladium or palladium alloy on the nickel layer.

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METAL COVER FOR CERAMIC PACKAGE AND METHOD OF MAKING SAME

Background of the Invention

1. Field of the Invention

This invention relates to a sealing cover which is particularly suitable for sealing ceramic packages for semiconductor devices, and to a method of producing the same.

2. Description of the Prior Art

The use of ceramic packages for semiconductor devices is well-known. Typically, such a package includes a ceramic container to which the cover must be sealed. Sealing covers, also known as "lids," of the type used in connection with containers for semiconductor devices are well known and typically include one or more layers of gold, often of substantial thickness, to aid in corrosion resistance as well as to provide for electrical connection of leads. Such covers are not only expensive but also introduce a possible health hazard, since cyanide solutions are often used in gold plating.

The present invention is directed to a novel sealing cover, and to a method of making same, which avoids or at least substantially reduces the use of gold, thus lowering cost and reducing potential health hazards by eliminating or greatly minimizing gold plating. By eliminating or

minimizing use of gold, material and manufacturing costs related to the production of lids for semiconductor packages can be significantly lowered. In accordance with the present invention, a sealing cover is provided which is not only economical because it replaces gold with palladium, but is also of sufficiently high quality to pass standard tests for temperature cycling and thermal shock as well as resistance to corrosion in a salt atmosphere.

Although use of palladium in the manufacture of sealing covers is known, such use has been primarily limited to palladium in the form of palladium-silver paste applied to ceramic lids. This use merely takes advantage of the ability of palladium to fuse to ceramic in paste form. However, even in such uses only small quantities of palladium paste are employed, generally around the perimeter of the cover, and the use of palladium in this manner does not materially reduce or affect the overall manufacturing costs.

Miyoshi, et al. U.S. Patent No. 4,640,436 has suggested the use of a coating of gold, palladium, silver or platinum on a solder ring to assist in diffusion bonding of the solder to the lid. In this case, the lid is plated with "a material of high solderability" such as gold. In Levine U.S. Patent Nos. 4,835,067 and 4,666,796, it is suggested to use palladium as a solderable coating on a metal lid as two distinct layers of palladium with a layer of a more reactive metal sandwiched between the two palladium layers. Patentee provides this structure to cancel the galvanic effect that the noble top layer would normally have on the iron-based substrate to which the layers are applied to avoid a possible "short circuit" created if the iron and gold become connected through pinholes in an intermediate layer.

The present invention differs from the prior art, and in particular the disclosures in the Levine patents, in that the present invention involves a metallic cover,

preferably with an iron-alloy core, and not a ceramic cover. Therefore, there is no need to coat the solder with palladium. The new sealing cover employs separate distinct layers without alternating the layers according to the EMF value of the coatings and only a single palladium-containing layer is employed. Surprisingly, the relatively simple construction of the cover of the present invention still imparts sufficient corrosion resistance in salt atmospheres while retaining its solderability, but at a substantially reduced cost over the gold-containing sealing covers heretofore known.

Summary of the Invention

In accordance with the invention, there is provided a metallic cover for hermetically sealing a semiconductor device package by soldering, which includes a substrate comprising a core of iron alloy, a first layer on the core which comprises nickel or nickel alloy, and a second layer on the first layer which comprises palladium or palladium alloy. To provide a cover which resembles those currently used, a coating of gold may be applied as an outer layer, but such a layer would be significantly thinner than that conventionally used. However, in many applications the layer of gold may be eliminated altogether without adversely affecting the desirable characteristics of the cover. The sealing cover of the invention may be made by providing a core of an iron alloy, such as iron-nickel alloy, applying a first layer comprising a nickel or nickel alloy onto the core and then applying a second layer comprising palladium or palladium alloy onto the first layer. Optionally, a final thin coating of gold may be applied onto the second layer.

A semiconductor device package may be assembled using a cover as described by soldering it to a ceramic enclosure having a semiconductor device therein to hermetically seal the package, with a gold-free solder selected from the group consisting of solders containing

at least one of lead, tin, silver, indium, bismuth, palladium, platinum and antimony, and which has a melting point in the range of from about 220°C to 300°C to avoid exposing the semiconductor device therein to elevated temperatures that might damage the device. The solder may be incorporated as a solder preform of suitable configuration. In this manner, a soldered hermetically sealed semiconductor package may be assembled using the sealing cover and method previously described.

Brief Description of the Drawings

FIG. 1 is a schematic cross-sectional view of a sealing cover showing a metallic core over which is applied a nickel-containing coating and a final gold layer over the nickel-coated core; and

FIG. 2 is a schematic representation of a sealing cover in accordance with the invention.

Detailed Description of the Invention

In the sealing cover construction described in FIG. 1, the final layer consists of a substantially thick layer of gold. If it is possible to reduce the thickness of the gold coating or eliminate it altogether, while retaining the required characteristics of corrosion-resistance, etc. a significant reduction in manufacturing costs would occur. This is accomplished by the cover described in FIG. 2, which is an example of the invention wherein a metallic core is coated with a nickel-containing material, but a palladium-containing layer is applied onto the nickel layer. The use of palladium or a palladium alloy in this manner avoids the need for a thick outer layer of gold and, for many applications, allows the gold layer to be omitted altogether. The term "palladium alloy" as used herein refers to an alloy in which palladium is a major constituent and present in an amount of at least about 30 wt.%.

In accordance with the presently preferred embodiment of the invention, a suitable metallic core, such as one made of iron-nickel alloy, known as "Alloy 42," "Alloy 45" or "Alloy 46" or the alloy known as "Kovar," may be provided. Alloys 42, 45 and 46 refer to compositions containing 42, 45 and 46 wt.% nickel, respectively. The particular composition of the core is not critical to the success of the cover of the invention and any iron-based alloy may be used for this purpose provided similar thermal expansion characteristics to ceramic is maintained.

A first layer of nickel or nickel alloy is applied to the core. The nickel-containing material may be applied as an electrolytic or "electroless" coating. Presently, an electrolytic nickel-containing coating is preferred, because it appears to provide good corrosion resistance and economical and repeatable manufacture process. In lieu of a nickel or nickel alloy, a first layer of tin, silver, cadmium, indium, lead, copper, cobalt, ruthenium,

iridium, zinc, or their alloys, may be employed. However, it has been determined that nickel and nickel alloys are preferred for their combination of cost, relative ease of application and resistance to corrosion.

The thickness of the first layer is very important in producing a sealing cover with desirable properties. It has been determined that the thickness of the nickel/nickel-alloy layer should be in the range of 100 to 800 μin. Although performance characteristics equal to that obtained with present technology can be achieved with as little as 100 μin, a cover with superior properties is not achieved until the minimum thickness of the nickel/nickel-alloy layer is in the range of 400 to 600 μin. The nominal thickness of this layer is advantageously about 500 μin.

As a second layer, it is important to use a layer of palladium or palladium alloy (as defined previously), and in particular, a palladium-nickel alloy. The most preferred composition presently is an alloy of about 80% palladium and about 20% nickel; however, alloys of at least about 30 wt.% palladium, balance nickel, silver or tin, are also particularly advantageous. In lieu of palladium and palladium alloys as aforesaid, however, it may be possible to use tin, platinum, silver, cadmium, indium, cobalt, lead, rhodium, ruthenium, iridium, or their alloys, and alloys of palladium with the foregoing. The thickness of the palladium-containing layer is not as critical as the thickness of the first layer to achieving desirable properties in the sealing cover. However, it has been determined that the palladium-containing layer should be present in a range of from 10 μin to 100 μin for maximum performance. Although performance characteristics equal to covers made with present technology could be achieved with as little as 10 μin, if the first layer is sufficiently thick, i.e., at least 400 to 600 μin of electrolytic nickel, superior performance may be achieved with a palladium-containing layer in the range of 20 to

60 μin. The improvement in performance of a cover employing a second layer of palladium-containing alloy is believed to be related to the statistical probability that each successive layer of plating will cover over porosity defects in the lower layer. Even though each such successive layer may have its own channel sites, the probability that defect sites will coincide with defects in other layers is very small. Palladium and palladium-containing alloys are preferred because of their excellent solderability characteristics and the ability of such materials to supplement the ability of the first layer to minimize pinhole pores which create paths between the iron-containing core and the surrounding, possibly corrosive, atmosphere.

Optionally, a coating of gold may be applied to the palladium-containing layer to provide an outer-surface appearance resembling sealing covers currently in use, which would improve the acceptability of the sealing cover in the marketplace. Some additional advantage may result from the application of the thin layer of gold by assisting tack welding of a preform to the lid. Substitutes for gold in this application may include tin, palladium, platinum, silver, cadmium, indium, cobalt, lead, rhodium, ruthenium, indium, and their alloys.

Desirably, the gold layer is present in the range of from 0 to less than 50 μin. Performance characteristics equal to covers made with present technology can be achieved without the gold layer if the second layer is a palladium-containing material of sufficient thickness, e.g., at least 50 μin, and the first layer is a nickel-containing layer also of sufficient thickness, e.g., at least 500 μin. As an example, superior performance may be achieved with a nominal gold thickness of 10 μin, which is believed sufficient to enhance solderability and cover pinhole pores which may be present in the first and/or second layers.

In order to determine the optimum combinations of materials to function as the layers in the above-described sealing cover, the following combinations of plating solutions and coatings were investigated as potential replacements for the standard nickel-and-gold-plated lid to determine if they may be used to produce a sealing cover that exhibits the same functional characteristics but at reduced cost. Obviously, the combinations including gold are more expensive than the gold-free combinations. The materials investigated appear in Table 1.

TABLE I

Sample I.D.	Metallization	Thickness
A1	Matte Sulfamate Nickel	(250 μin)
	Pure Gold	(50 μin)
A2	Matte Sulfamate Nickel	(250 μin)
	Palladium/Nickel	(50 μin)
A3	Matte Sulfamate Nickel	(250 μin)
	Palladium/Nickel	(50 μin)
	Pure Gold	(7 μin)
A4	Matte Sulfamate Nickel	(250 μin)
	Tin/Zinc	(100 μin)
B1	Electroless Nickel	(250 μin)
	Pure Gold	(50 μin)
B2	Electroless Nickel	(250 μin)
	Palladium/Nickel	(50 μin)
B3	Electroless Nickel	(250 μin)
	Palladium/Nickel	(50 μin)
	Pure Gold	(7 μin)
B4	Electroless Nickel	(250 μin)
	Tin/Zinc	(100 μin)
C1	Electroless Nickel	(150 μin)
	Matte Sulfamate Nickel	(100 μin)
	Pure Gold	(50 μin)
C2	Electroless Nickel	(150 μin)
	Matte Sulfamate Nickel	(100 μin)
	Palladium/Nickel	(50 μin)
C3	Electroless Nickel	(150 μin)
	Matte Sulfamate Nickel	(100 μin)
	Palladium/Nickel	(50 μin)
	Pure Gold	(7 μin)
C4	Electroless Nickel	(150 μin)
	Matte Sulfamate Nickel	(100 μin)
	Tin/Zinc	(100 μin)
D1	Semi-bright Sulfamate Ni	(125 μin)
	Matte Sulfamate Nickel	(125 μin)
	Pure Gold	(50 μin)

1	D2	Semi-bright Sulfamate Ni	(125 μin)
		Matte Sulfamate Nickel	(125 μin)
		Palladium/Nickel	(50 μin)
	D3	Semi-bright Sulfamate Ni	(125 μin)
		Matte Sulfamate Nickel	(125 μin)
		Palladium/Nickel	(50 μin)
5		Pure Gold	(7 μin)
	D4	Semi-bright Sulfamate Ni	(125 μin)
		Matte Sulfamate Nickel	(125 μin)
		Tin/Zn	(100 μin)
	E1	Palladium/Nickel	(10 μin)
		Matte Sulfamate Nickel	(240 μin)
		Pure Gold	(50 μin)
10	E2	Palladium/Nickel	(10 μin)
		Matte Sulfamate Nickel	(140 μin)
		Palladium Nickel 80/20	(30 μin)
	E3	Palladium/Nickel	(10 μin)
		Matte Sulfamate Nickel	(140 μin)
		Palladium Nickel 80/20	(30 μin)
		Pure Gold	(7 μin)
	E4	Palladium/Nickel	(10 μin)
15		Matte Sulfamate Nickel	(10 μin)
		Tin/Zinc	(100 μin)
	F1	Electroless Nickel	(500 μin)
		Pure Gold	(50 μin)
	F2	Electroless Nickel	(500 μin)
		Palladium/Nickel	(50 μin)
	F3	Electroless Nickel	(500 μin)
20		Palladium/Nickel	(50 μin)
		Pure Gold	(7 μin)
	F4	Electroless Nickel	(500 μin)
		Tin/Zinc	(100 μin)
	G3	Matte Sulfamate Nickel	(500 μin)
		Palladium/Nickel	(50 μin)
		Pure Gold	(7 μin)
	H3	Electroless Nickel	(500 μin)
25		Palladium/Nickel	(50 μin)
		Pure Palladium	(10 μin)
	H4	Electroless Nickel	(500 μin)
		Pure Palladium	(50 μin)

Of the foregoing, the samples which outperformed 30 covers made by present technologies with respect to salt atmosphere corrosion resistance were:

F2	Electroless Nickel	(500 μin)
	Palladium/Nickel	(50 μin)
F3	Electroless Nickel	(500 μin)
35	Palladium/Nickel	(50 μin)
	Pure Gold	(7 μin)

	G3	Matte Sulfamate Nickel	(500 μin)
		Palladium/Nickel	(50 μin)
		Pure Gold	(7 μin)
	H3	Matte Sulfamate Nickel	(500 μin)
		Palladium/Nickel	(40 μin)
		Pure Palladium	(10 μin)
	H4	Matte Sulfamate Nickel	(500 μin)
		Pure Palladium	(50 μin)

From investigation of the above combinations, it was determined that the materials of samples G3 and A3 produced the most satisfactory results. Therefore, these samples were scaled up to normal production-size baths of 25 gallons and production runs were conducted to confirm the improvements obtained. The following example describes a typical plating sequence and the plating parameters of each step of the preferred process. The load size in each case was 300g of 0.605 x 0.605 lids, using a standard barrel, Sterling Model 46.

Step 1 ALKALINE ELECTRO-CLEANER

Product	Alkaline soap cleaner, e.g., Micel's X-Cel-133
Concentration	0.5 lbs/gal
Solution temperature	150°F
Current	Cathodic at 4 volts
Exposure time	10 minutes

Step 2 D.I. WATER RINSE

Exposure time	10 minutes

Step 3 ACID ACTIVATOR

Hydrochloric acid	30% by volume
Solution temperature	Ambient
Exposure time	10 minutes

Step 4 D.I. WATER RINSE

Exposure time	2 minutes

Step 5 *Alternate A*
ELECTROLYTIC NICKEL

Product	Matte sulfamate nickel
Nickel concentration	0.5 lbs/gal
Nickel bromide	2.0 oz/gal
Boric acid	4.0 oz/gal
pH	4.3
Solution temperature	130°F
Current	12 amperes
Deposition Rate	90 μin/hour

Step 5 *Alternate B*
MID-PHOS ELECTROLESS NICKEL

Product	Mid-Phos electroless nickel
Nickel concentration	0.5 lbs/gal
pH	5.0
Solution temperature	150°F
Deposition Rate	350 μin/hour

Step 6 D.I. WATER RINSE

Exposure time	2 minutes

Step 7 ACID ACTIVATOR

Hydrochloric acid	30% by volume
Solution temperature	Ambient
Exposure time	10 minutes

Step 8 D.I. WATER RINSE

Exposure time	1 minute

Step 9 PALLADIUM/NICKEL ALLOY

Product	80% Pd - 20% Ni
Palladium concentration	0.5 lbs/gal
Nickel concentration	2.0 oz/gal
Deposit modifier	1.0% by vol
Stress reducer	1.0% by vol
pH	8.5
Solution temperature	90°F
Current	6.1 amperes
Deposition Rate	30 μin/hour

Step 10 *Alternate A*
PURE GOLD

Product	Mil. Spec. G-45204, Type 3, Grade A. pure gold
Gold concentration	0.75 oz/gal
Additive T concentration	1.0% by vol
Stabilizer	12% by vol
Baume	16°
pH	6.8
Solution temperature	110°F
Current	1 amperes
Deposition Rate	30 μin/hour

Step 10 *Alternate B*
PURE PALLADIUM

Product	100% Pd.
Palladium concentration	10 g/l
Additive concentration	50 g/l
Brightener	0.5% by volume
Baume	16°
pH	9.5
Solution temperature	120°F
Current	1 amperes
Deposition Rate	30 μin/hour

Evaluation of sealing covers produced in accordance with the invention has indicated that the preferred material for the core of the cover is an iron-nickel alloy, such as Alloy 42, Alloy 45, Alloy 46 or Kovar. The preferred composition of the first layer is electrolytic or electroless nickel and/or nickel alloy, with electrolytic nickel and/or nickel alloy considered most advantageous. Preferably, the palladium-containing layer is formed of a palladium-nickel alloy, optimally 80% palladium and 20% nickel, or 30 to 100% palladium with silver or tin.

The sealing cover is hermetically sealed to the ceramic package by soldering. Advantageously, to reduce costs, it is desirable to employ a gold-free or substantially gold-free solder for this purpose. It has been determined that the gold-free solder should be one selected from the group consisting of solders containing

at least one of lead, tin, silver, palladium platinum, indium, bismuth and antimony, but which have a melting point in the range of about 220°C to 300°C. These relatively low melting-point solders are additionally preferred so as to avoid the necessity of exposing the semiconductor device within the package to elevated temperatures, such as might possibly injure the semiconductor. More advantageously, preferred compositions include solders containing in wt.% about 75% tin, about 20% silver and about 5% antimony; solders containing about 84.5% lead, 5.5% indium, 5% tin, 3% antimony and 2% silver; and solders containing up to about 95% lead, preferably not less than 90% lead, up to about 5% palladium and which may additionally include up to about 5% silver, up to about 5% bismuth, up to about 5% antimony, and up to about 5% gold or a mixture of gold and tin having up to about 5% gold and up to about 2% tin. Other useful solders include 95% Pb-5% Pt.

To further illustrate solders useful in accordance with the present invention, 12 solder compositions shown in the following table have been prepared:

solder comp'n	Pb	Sn	Ag	In	Bi	Sb	Pt	Pd	Au
1		75.0	20.0			5.0			
2		80.0	10.0			10.0			
3	84.5	5.0	2.0	5.5		3.0			
4	88.0	4.5	2.5	5.0					
5	95.0						5.0		
6	95.0							5.0	
7	90.0	1.0						5.0	4.0
8	93.0	0.5						5.0	1.5
9	90.0		5.0					5.0	
10	90.0				5.0			5.0	
11	90.0			5.0				5.0	
12	93.0					2.0		5.0	

Ceramic packages with sealing covers as described herein have been found to be capable of passing Mil. Std. 883C, Method 1010 for Test Condition C, 1,000 x temperature cycles and thermal shock testing. In addition, the essentially three-layer cover described herein is also able to pass salt-atmosphere testing, is very solderable and cosmetically identical to the lid described in Mil-M-38510G (50 to 350 μin nickel under 50 to 225 μin gold), with all the same physical properties, but at a much reduced cost.

Resistance to corrosion in a salt atmosphere is generally measured as a percentage of surface area which is corroded. Sealing covers of the present invention have less than 1% corrosion and preferably, less than 1/2%

corrosion, in terms of surface area, as determined according to Mil-Std-883, Method 1009.9, Condition A.

In the conventional lid combining a first nickel layer on an iron-nickel core and an outer gold layer, the first layer is nominally 250 μin and the gold layer is 50 μin. The usual test to measure salt atmosphere corrosion resistance involves exposing 25 test pieces at a time. Corrosion resistance of convention covers exhibit test results showing < 1% surface area corrosion, with an average of about 0.25% surface area corrosion. In contrast, comparable tests of 25 pieces of 500 μin Ni on an iron-nickel alloy core with 40 μin Pd-Ni alloy and 5 μin Au results in < 0.5% surface area corrosion and an average of about 0.1%.

The following is an example of one preferred embodiment. A core of "Alloy 42" is spot welded to a solder ring. Three steps are used to fabricate a complete lid.

A. Plated lid production.

B. Solder ring production and punching.

C. Attachment of the solder ring to the plated lid.

Each process is described in detail below.

A. Plated Lid Production

Alloy 42 (Fe 58%, Ni 42%) is rolled into sheets 0.010" to 0.015" thick, and annealed into a state making it suitable for punching (typically 95,000 psi tensile strength). The sheet is slit into coils wide enough to make them easily punched through a progressive die set.

Using standard technology this material is then punched into sizes suitable for sealing onto ceramic packages. Typical sizes include:

.250" x .375" x 0.010"

.505" x .505" x 0.010"

.860" x .860" x 0.015"

The punched squares may then be deburred chemically or mechanically to clean up any rough edges that may result from metal shearing.

The cleaned and deburred lids may than be loaded into a plating barrel for degreasing, oxide removal, and electroplating of all desired layers. One barrel of low cost lids were plated using the following sequence:

1. A Sterling System 6" x 12" plating barrel was loaded about 30% full with .605" x .605" x 0.010" alloy 42 squares which had been previously punched and deburred in the manner described above.

2. This barrel was plated with nickel, palladium-nickel and gold using the following sequence:

   a. Electroclean at 5 volts anodic for 5 minutes;
   b. Rinse for at least 5 minutes;
   c. Descale in acid blend for 5 minutes;
   d. Rinse for 2 minutes;
   e. Plate in Sulfamate Nickel for ample time to deposit 500 μin;
   f. Rinse for 5 minutes;
   g. Acid activate in 5% HCl (optional);
   h. Plate in Pd-Ni for ample time to deposit 40 μin;
   i. Rinse for 5 minutes;
   j. Plate in a high adhesion pure gold bath for ample time to deposit 5 μin 99.9% pure gold;
   k. Rinse for 10 minutes in warm cascading deionized water; and
   l. Dry in TDFC Freon dryer or suitable substitute.

3. Lids electroplated in the manner described will routinely pass the following tests:

   a. A 450°C five-minute bake in air;
   b. A corrosion test permit std 883c., method 1009 condition A; and
   c. A visual test for stains, blisters, or poor adhesion.

B. Solder Ring Production and Punching

A predetermined quantity 99.99% pure lead is brought to its melting point in a bottom draw continuous caster. To the molten lead is added 5.0 wt.% 99.99% pure palladium in powder form. After allowing ample time for the mixture to alloy, the metal is cast continuous style through a 0.200" x 2.000" die. (Other size die are also suitable.)

The resulting 0.200" x 2.000" piece is rolled down to a thickness of 0.0021" +/- 0.003" over 12 passes at room temperature. A petroleum based oil is used as a lubricant.

After removal of the rolling oil with naphtha and methylene chloride, the clean strip is punched into "window frame" shapes 0.0021" thick x 0.605" OD x 0.505" ID. A compound punching die set is used, and although the material deforms easily, several thousand pieces are made in this manner.

A final wash in Freon or another suitable solvent is optional at this stage, although it has been found not to be necessary.

C. Attachment of the Solder Ring to the Plated Lid

Appropriate tooling for fastening the solder window frames of step B to the plated alloy 42 lids of step A is performed by methods known to the trade and typically produced by specialty manufacturers, usually by resistance welding.

The tooling used for this work is generally insulating platform with 8 pins arranged to hold the lid and solder ring in alignment. Arranged 0.025" in from each corner in the block is an electrode extending 0.005" out of the block.

By clamping the assembly in place from above, it is possible to spot weld the lid to the solder by passing a high current through the electrodes.

This lid-solder combination is the finished product which may be used to hermetically seal a silicon die into a ceramic package.

In view of the foregoing description, it is apparent that various changes and modifications may be made without departing from the invention. Accordingly, the scope of the invention should be limited only by the appended claims.

WHAT IS CLAIMED IS:

1. A solderable metallic cover for hermetically sealing a package containing a semiconductor device comprising a core of iron or iron-nickel alloy, a first layer on said core comprising nickel, tin, silver, cadmium, indium, lead, copper, cobalt, ruthenium, iridium, zinc, and alloys thereof, and a second layer on said first layer comprising palladium, tin, platinum, silver, cadmium, indium, cobalt, lead, rhodium, ruthenium, iridium, and alloys thereof, and a layer of gold on said second layer of a thickness of 0 to 50 μin.

2. A solderable metallic cover for hermetically sealing a package containing a semiconductor device comprising a core of iron or iron-nickel alloy, a first layer on said core comprising nickel or nickel alloy, and a second layer on said first layer comprising palladium or palladium alloy and a layer of gold on said second layer of a thickness of 0 to 50 μin.

3. A cover according to claim 2 wherein said substrate comprises one of Alloy 42, Alloy 45, Alloy 46 or Kovar.

4. A cover according to claim 2 wherein said first layer comprises one from the group consisting of electrolytic and electroless nickel and alloys of nickel of a thickness of 100 to 800 μin.

5. A cover according to claim 4 wherein said first layer is 400 to 600 μin.

6. A cover according to claim 2 wherein said second layer comprises at least about 30 wt.% palladium, the balance nickel, silver or tin.

7. A cover according to claim 2 wherein said second layer comprises an alloy of palladium and nickel.

8. A cover according to claim 6 wherein said second layer comprises 10 to 100 μin of one from the group consisting of palladium and alloys of palladium.

9. A cover according to claim 8 wherein said second layer comprises 20 to 60 μin.

10. A cover according to claim 6 wherein said second layer comprises an alloy of about 80% palladium and about 20% nickel, by weight.

11. A method of assembling a semiconductor device package comprising soldering a cover according to claim 1 to a ceramic enclosure having a semiconductor device therein to hermetically seal said package with a gold-free solder selected from the group consisting of solders containing at least one of Pb, Sn, Ag, In, Bi, Pd, Pt and Sb, and which has a melting point in the range of from about 220°C to 300°C.

12. A method according to claim 11 wherein said solder comprises in wt.% about 75% Sn, about 20% Ag and about 5% Sb.

13. A method according to claim 11 wherein said solder comprises in wt.% about 84.5% Pb, about 5.5% In, about 5% Sn, about 3% Sb and about 2% Ag.

14. A method according to claim 11 wherein said solder comprises about 95% Pb and about 5% Pd.

15. A method according to claim 11 wherein said solder comprises up to about 95% Pb, up to about 5% Pd, up to about 5% Ag, up to about 5% Bi, up to about 5% Sb, up

to 5% Au, and up to about 7% of a mixture of Au and Sn having up to about 5% Au and up to 2% Sn.

16. A method of assembling a semiconductor device package comprising soldering a cover according to claim 2 to a ceramic enclosure having a semiconductor device therein to hermetically seal said package with a gold-free solder selected from the group consisting of solders containing at least one of Pb, Sn, Ag, In, Bi, Pd, Pt and Sb, and which has a melting point in the range of from about 220°C to 300°C.

17. A method according to claim 16 wherein said solder comprises in wt.% about 75% Sn, about 20% Ag and about 5% Sb.

18. A method according to claim 16 wherein said solder comprises in wt.% about 84.5% Pb, about 5.5% In, about 5% Sn, about 3% Sb and about 2% Ag.

19. A method according to claim 16 wherein said solder comprises about 95% Pb and about 5% Pd.

20. A method according to claim 16 wherein said solder comprises up to about 95% Pb, up to about 5% Pd, up to about 5% Ag, up to about 5% Bi, up to about 5% Sb, up to 5% Au, and up to about 7% of a mixture of Au and Sn having up to about 5% Au and up to 2% Sn.

21. A method of making a cover for a ceramic semiconductor package comprising:

providing a core comprising iron or iron-nickel alloy;

applying onto said core a first layer comprising nickel, tin, silver, cadmium, indium, lead, copper, cobalt, ruthenium, iridium, zinc, and alloys thereof; and

applying a second layer onto said first layer comprising palladium, tin, platinum, silver, cadmium, indium, cobalt, lead, rhodium, ruthenium, iridium, and alloys thereof.

22. A method according to claim 21 further comprising applying a layer of gold onto said second layer.

23. A method according to claim 21 wherein said core comprises one of Alloy 42, Alloy 45, Alloy 46 and Kovar.

24. A method according to claim 21 wherein said first layer comprises one from the group consisting of electrolytic and electroless nickel and alloys of nickel and is applied in a thickness of 100 to 800 μin.

25. A method according to claim 22 wherein said second layer is applied in a thickness of 20 to 60 μin.

26. A method according to claim 21 wherein said second layer comprises an alloy of palladium and nickel.

27. A method according to claim 24 wherein said second layer is applied in a thickness of 10 to 100 μin.

28. A method according to claim 25 wherein said second layer is applied in a thickness of 20 to 60 μin.

29. A method according to claim 25 wherein said second layer comprises an alloy of 80% palladium and 20% nickel, by weight.

30. A method according to claim 21 wherein said second layer comprises at least about 30 wt.% Pd, the balance, Ni, Sn or Ag.

31. A method of making a cover for a ceramic semiconductor package comprising:

providing a core comprising iron or iron-nickel alloy;

applying onto said core a first layer comprising nickel or nickel alloy; and

applying a second layer onto said first layer comprising palladium or palladium alloy.

32. A method according to claim 31 further comprising applying a layer of gold onto said second layer.

33. A method according to claim 31 wherein said core comprises one of Alloy 42, Alloy 45, Alloy 46 and Kovar.

34. A method according to claim 31 wherein said first layer comprises one from the group consisting of electrolytic and electroless nickel and alloys of nickel and is applied in a thickness of 100 to 800 μin.

35. A method according to claim 31 wherein said second layer comprises an alloy of palladium and nickel.

36. A method according to claim 31 wherein said second layer is applied in a thickness of 20 to 60 μin.

37. A method according to claim 31 wherein said second layer is applied in a thickness of 10 to 100 μin.

38. A method according to claim 31 wherein said second layer is applied in a thickness of 20 to 60 μin.

39. A method according to claim 31 wherein said second layer comprises an alloy of 80% palladium and 20% nickel, by weight.

40. A soldered, hermetically sealed semiconductor package comprising a ceramic enclosure having a semiconductor device therein and a cover soldered to the ceramic enclosure to hermetically seal said ceramic enclosure, said cover including a core comprising an iron or iron-nickel alloy, a first layer on said substrate comprising nickel, tin, silver, cadmium, indium, lead, copper, cobalt, ruthenium, iridium, zinc, and alloys thereof, a second layer on said first layer comprising palladium, tin, platinum, silver, cadmium, indium, cobalt, lead, rhodium, ruthenium, iridium, and alloys thereof, said cover being soldered to said ceramic enclosure with a gold-free solder selected from the group consisting of solders containing at least one of Pb, Sn, Ab, In, Bi, Pd, Pt and Sb, and which has a melting point in the range of from about 220°C to 300°C.

41. A package according to claim 40 wherein said cover further comprises a coating of gold on said second layer.

42. A soldered, hermetically sealed semiconductor package according to claim 40 wherein said core comprises one of Alloy 42, Alloy 45, Alloy 46 and Kovar.

43. A soldered, hermetically sealed semiconductor package according to claim 40 wherein said first layer comprises 100 to 800 μin of one from the group consisting of electrolytic and electroless nickel and alloys of nickel.

44. A soldered, hermetically sealed semiconductor package according to claim 40 wherein said first layer is 400 to 600 μin.

45. A soldered, hermetically sealed semiconductor device according to claim 40 wherein said second layer

comprises at least about 30 wt.% Pd, the balance at least one from the group consisting of Ni, Ag and Sn.

46. A soldered, hermetically sealed semiconductor package according to claim 41 wherein said second layer comprises 10 to 100 μin of one from the group consisting of palladium and alloys of palladium.

47. A soldered, hermetically sealed semiconductor package according to claim 45 wherein said second layer comprises an alloy of palladium and nickel.

48. A soldered, hermetically sealed semiconductor package according to claim 46 wherein said second layer comprises an alloy of 80% palladium and 20% nickel, by weight.

49. A soldered, hermetically sealed semiconductor package according to claim 46 wherein said second layer comprises 20 to 60 μin of an alloy of palladium and nickel.

50. A soldered, hermetically sealed semiconductor package according to claim 41 wherein said solder comprises in wt.% about 75% Sn, 20% Ag and 5% Sb.

51. A soldered, hermetically sealed semiconductor package according to claim 41 wherein said solder comprises in wt.% about 84.5% Pb, 5.5% In, 5% Sn, 3% Sb and 2% Ag.

52. A soldered, hermetically sealed semiconductor package according to claim 41 wherein said solder comprises about 95 wt.% Pb and about 5 wt.% Pd.

53. A soldered, hermetically sealed semiconductor package according to claim 41 wherein said solder

comprises up to about 95% Pb, up to about 5% Pd, up to about 5% Ag, up to about 5% Bi, up to about 5% Sb, up to 5% Au, and up to about 7% of a mixture of Au and Sn having up to about 5% Au and up to 2% Sn.

54. A soldered, hermetically sealed semiconductor package comprising a ceramic enclosure having a semiconductor device therein and a cover soldered to the ceramic enclosure to hermetically seal said ceramic enclosure, said cover including a core comprising an iron or iron-nickel alloy, a first layer on said substrate comprising nickel or nickel alloy, a second layer on said first layer comprising palladium or palladium alloy, said cover being soldered to said ceramic enclosure with a gold-free solder selected from the group consisting of solders containing at least one of Pb, Sn, Ag, In, Pd, Pt, Bi and Sb, and which has a melting point in the range of from about 220°C to 300°C.

55. A package according to claim 54 wherein said cover further comprises a coating of gold on said second layer.

56. A soldered, hermetically sealed semiconductor package according to claim 54 wherein said core comprises one of Alloy 42, Alloy 45, Alloy 46 or Kovar.

57. A soldered, hermetically sealed semiconductor package according to claim 54 wherein said first layer comprises 100 to 800 μin of one from the group consisting of electrolytic and electroless nickel and alloys of nickel.

58. A soldered, hermetically sealed semiconductor package according to claim 56 wherein said first layer is 400 to 600 μin.

59. A soldered, hermetically sealed semiconductor package according to claim 54 wherein said second layer comprises at least about 30 wt.% Pd, the balance at least one of Ni, Ag and Sn.

60. A soldered, hermetically sealed semiconductor package according to claim 54 wherein said second layer comprises 10 to 100 μin of one from the group consisting of palladium and alloys of palladium.

61. A soldered, hermetically sealed semiconductor package according to claim 58 wherein said second layer comprises an alloy of palladium and nickel.

62. A soldered, hermetically sealed semiconductor package according to claim 60 wherein said second layer comprises an alloy of 80% palladium and 20% nickel, by weight.

63. A soldered, hermetically sealed semiconductor package according to claim 60 wherein said second layer comprises 20 to 60 μin of an alloy of palladium and nickel.

64. A soldered, hermetically sealed semiconductor package according to claim 54 wherein said solder comprises in wt.% about 75% Sn, 20% Ag and 5% Sb.

65. A soldered, hermetically sealed semiconductor package according to claim 54 wherein said solder comprises in wt.% about 84.5% Pb, 5.5% In, 5% Sn, 3% Sb and 2% Ag.

66. A soldered, hermetically sealed semiconductor package according to claim 54 wherein said solder comprises in wt.% about 95% Pb and about 5% Pd.

67. A sealing cover consisting essentially of an iron and nickel alloy core, a 400 μin thick first layer of material from the group consisting of nickel, tin, silver, cadmium, indium, lead, copper, cobalt, ruthenium, iridium, zinc, and alloys thereof, a 20-60 μin second layer of a material from the group consisting of palladium, tin, platinum, silver, cadmium, indium, cobalt, lead, rhodium, ruthenium, iridium, and alloys thereof and a layer of 0 to 15 μin of gold on the second layer.

68. A sealing cover consisting essentially of an iron and nickel alloy core, a 400 μin thick first layer of material from the group consisting of nickel and nickel alloys, a 20-60 μin second layer of a material from the group consisting of palladium and palladium-nickel alloys and a layer of 0 to 15 μin of gold on the second layer.

69. A method of making a sealing cover comprising providing a core of an alloy of iron and nickel, applying a first layer to the core comprising nickel or nickel alloy of 100 to 800 μin thickness and applying a second layer onto the first layer of palladium or palladium-nickel alloy of 10 to 100 μin thickness.

70. A method according to claim 68 further comprising applying a layer of gold of 0 to 15 μin thickness onto the second layer.

71. A method according to claim 68 wherein said first layer is applied as a layer of 400 to 600 μin thickness.

72. A method according to claim 68 wherein said second layer is applied as a layer of 20 to 60 μin thickness.

73. A method according to claim 68 wherein said first layer is electrolytic nickel.

74. A method according to claim 68 wherein said second layer is applied as a layer of at least 30% palladium, the balance nickel.

AMENDED CLAIMS

[received by the International Bureau on 6 September 1994 (06.09.94);
original claim 3 amended;
other claims unchanged (1 page)]

1. A solderable metallic cover for hermetically sealing a package containing a semiconductor device comprising a core of iron or iron-nickel alloy, a first layer on said core comprising nickel, tin, silver, cadmium, indium, lead, copper, cobalt, ruthenium, iridium, zinc, and alloys thereof, and a second layer on said first layer comprising palladium, tin, platinum, silver, cadmium, indium, cobalt, lead, rhodium, ruthenium, iridium, and alloys thereof, and a layer of gold on said second layer of a thickness of 0 to 50 μin.

2. A solderable metallic cover for hermetically sealing a package containing a semiconductor device comprising a core of iron or iron-nickel alloy, a first layer on said core comprising nickel or nickel alloy, and a second layer on said first layer comprising palladium or palladium alloy and a layer of gold on said second layer of a thickness of 0 to 50 μin.

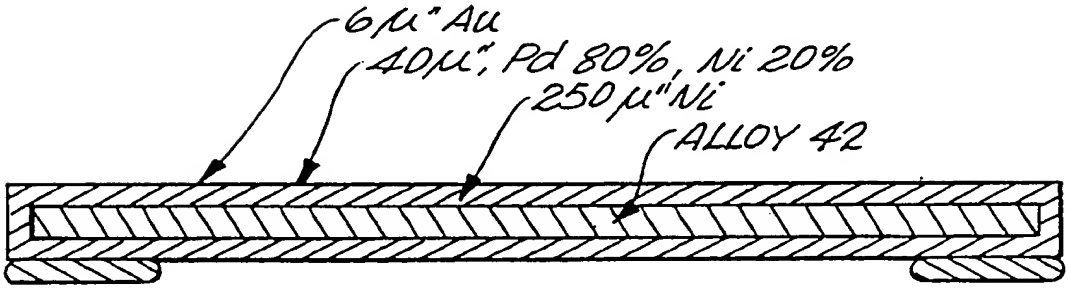
3. A cover according to claim 2 wherein said core comprises one of Alloy 42, Alloy 45, Alloy 46 or Kovar.

4. A cover according to claim 2 wherein said first layer comprises one from the group consisting of electrolytic and electroless nickel and alloys of nickel of a thickness of 100 to 800 μin.

5. A cover according to claim 4 wherein said first layer is 400 to 600 μin.

6. A cover according to claim 2 wherein said second layer comprises at least about 30 wt.% palladium, the balance nickel, silver or tin.

Fig. 2 EXAMPLE OF NEW LID



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/03788

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 23/02, 21/465; H05K 5/06; H01S 4/00

US CL :Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 174/52.2, 52.3, 52.4; 257/678, 699,704; 437/225, 245, 246; 29/592.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 5,045,639 (Liu et al.) 03 September 1991, Fig. 2	1
Y	US,A,4,842,961 (Basile et al.) 27 JUNE 1989, claims 1-15	1-74
Y	US,A,4,737,418 (Slattery) 12 APRIL 1988, Figs. 4-6	1-74
Y	US,A,4,666,796 (Levine) 19 MAY 1987, entire document	1-74
Y	US,A,4,835,067 (Levine) 30 MAY 1989, entire document	1-74
Y	US,A,4,640,438 Trevison et al.) 03 FEBRUARY 1987, Figs. 1-2	1-74

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
22 JUNE 1994

Date of mailing of the international search report
07 JUL 1994

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/03788

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A,4,640,436 (Miyoshi et al.) 03 FEBRUARY 1987,Figs. 1-3	1-74
Y	US,A,4,601,958 (Levine) 22 JULY 1986, entire document	1-74
Y	US,A,4,331,253 (Gordon et al.) 25 MAY 1982, col. 3, lines 1-49	1-74
Y	US,A,4,331,258 (Geschwind) 25 MAY 1982, entire document	1-74
Y	US,A,4,141,029 (DROMSKY) 20 february 1979, Fig. 3	1-74

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/03788

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

174/52.2, 52.3, 52.4; 257/678, 699,704; 437/225, 245, 246; 29/592.1

Fig. 2 EXAMPLE OF NEW LID